IN THE SPECIFICATION

Please amend Paragraphs [0023], [0042], and [0047] as follows:

[0023] Figure 1B depicts another flash memory array of the prior art that utilizes a local interconnect 160 that has been formed between the word line stacks 145 to contact the array source region 140 and function as a source local interconnect. In Figure 1B, as with Figure 1A, a bit line 150 has been formed and bit line contacts 155 couple the bit line 150 to the drain regions 135 of the array. The local source interconnects 160 of Figure 1B are typically formed by a standard process method in which, after patterning the word line stacks 145 and depositing the insulating layer 165, a dry etch is utilized to form a trench or contact hole in the insulating layer 165 on the array source region 140. The trench or contact hole is then filled with doped polysilicon or metal. A problem with this is that the typical dry etch utilized against the insulating layer 165 does not have very good selectivity against the portion of the insulator 165 used to form the sidewalls and cap layer of the word line stacks 145 (not shown) and can dangerously thin them. As the cap layer and sidewall dielectric insulates the source local interconnect supply line 160 from the word line stack 145, if it is too thin it can break down when erase voltages (which can be as high as 16v-20v) are applied to the array, causing failure of the memory device. As a result, an insulating ~~insulting~~ cap layer and the insulating sidewalls of the word line stacks 145 are over-designed to avoid this problem. As detailed in Figure 1B, the local interconnects 160 and their insulating sidewalls and cap layers limit the amount the array may be reduced in word line pitch size without reducing the critical insulation separation of the interconnect 160 and the adjacent word line stacks 145. The additional insulation layer margin has the effect of limiting the amount of word line pitch reductions to avoid dangerously thinning the insulation layer 165 between the word line stacks 145 and the deposited interconnects 160.

[0042] Once the stacks of Figure 2A are formed, a layer of dielectric material 275, such as TEOS (tetraethylorthosilicate) or silicon nitride, is then formed by a blanket deposition process over the patterned word line stacks 245 as shown in Figure 2B. The layer of dielectric material 275 is utilized to form the dielectric spacers 275 that separate and electrically insulate the word line stacks 245 from the local interconnect lines and contacts that are deposited later to connect to the drain ~~source~~ regions 235 and source ~~drain~~ regions 240.

[0047] In embodiments of the invention, by utilizing a low resistance polysilicon local interconnect the source interconnect 290 can extend over a much larger group of memory cells in addition to allowing the reduction in word line pitch. This configuration can facilitate array source interconnects extending 32 columns or more without coupling to an array ground. In addition, by utilizing a shallow junction for the source region 240, a smaller channel can be utilized in the memory array, thus facilitating a reduction in device size and a reduction in pitch. As described herein, a memory cell is a single floating-gate transistor formed of a word line 225, drain region 235, source region 240 and a channel region defined by the area interposed between the drain region 235 and source region 240. It is also noted that the formation of bit line contacts utilizing the techniques are disclosed herein. However, in forming bit line contacts, the area of dielectric and polysilicon exposed over the drain region will typically be in the form of a contact hole rather than a trench.